IN THE SPECIFICATION:

Kindly amend the paragraph starting on page 4, line 20 as follows:

D1

Figs. 10A-E ~~10A-C~~, 11, and 12 are detailed block diagrams of preferred register formats utilized at the I/O bridge of the present invention. ;

Kindly amend the paragraph starting on page 9, line 8 as follows.

In particular, for each port P0-P3 of the IO7 there is a POx_CTRL control register 800 of Fig. 7 having a plurality of fields. Figs. 10A-E ~~11A-C~~ are a detailed preferred format of ~~a~~ the POx_CTRL control register 1500. A POx_CTRL control register 800 is preferably disposed at each port P0-P3 of the IO7 and is written or set-up during initialization of the IO7. It may also be written or set-up during operation of the IO7. As shown, the POx_CTRL control register format 1500 is organized into a plurality of fields. An RM_TYPE field 1502 (Fig. 10B ~~10C~~) is preferably used, at least in part, to control a novel pre-fetch algorithm, which is disclosed in a co-pending patent serial no. 09/652,644 [_____], entitled, Adaptive Data Prefetch Prediction Algorithm, filed August 31, 2000 [_____]. Which application is hereby incorporated herein by reference. In particular, the RM_TYPE field 1502 controls the maximum

D2

D2 cont'd.

number of DMA engines that may be assigned to process a given transaction. The RM_TYPE field 1502 may be 2-bits long.

Kindly amend the paragraph starting on page 12, line 6 as follows:

D3

Specifically, as described above, each IO7 400 includes a POx_CTRL control register 1500 (Figs. 10A-E ~~11A-C~~) that contains information utilized by the IO7 400 when it is initialized. The POx_CTRL register 1500 preferably includes a UPE_ENG_EN field 1504 (Fig. 10C). The UPE_ENG_EN field 1504 preferably includes at least one bit for each DMA engine at the IO7 400. In the preferred embodiment, each IO7 400 has twelve DMA engines. Accordingly, the UPE_ENG_EN field 1504 has twelve DMA engine enable bits. Only UPE engines that are enabled in UPE_ENG_EN can be used to process DMA transactions. In this way a user can program the number of DMA engines (up to some maximum, e.g., twelve) that are enabled and run at a given IO7 400. If an EV7 processor 202 is to be hot swapped a user, operating through system software or firmware, preferably de-asserts all twelve DMA engine enable bits of the IO7 400 coupled to the EV7 202 that is to be removed. That is, the user sets all bits of the UPE_ENG_EN field 1504 of the respective POx_CTRL control register 1500 to "0". In response, the IO7 400 stops allocating DMA engines for new transactions, thereby stopping the IO7 400 from commencing new transactions. When a DMA

D3 contd. engine that was in use is subsequently disabled, it nonetheless completes the pending or existing transaction(s) that were assigned to it.